IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 3, 6, 7 and 10 in accordance with the following:

1. (currently amended) A timer adjusting system for adjusting timers of a plurality of processors in a multi-processor system, ~~comprising:~~ each processor including a generating circuit generating a time synchronous signal for the multi-processor system~~;~~, an output circuit outputting the time synchronous signal~~;~~, and an input circuit inputting the time synchronous signal ~~that is~~, said time adjusting system comprising:

a distributing circuit propagating the time synchronous signal output from the output circuit of one of the processors to all of the processors in the multi-processor system and ~~returns~~ returning the time synchronous signal to the input circuit of the one of the processors after being propagated in the multi-processor system;

a measuring circuit measuring a time ~~while~~ from when the output circuit of the one of the processors outputs the time synchronous signal ~~and~~ to when the input circuit of the one of the processors inputs the time synchronous signal; and

a synchronization circuit correcting time information of one or more timers of the plurality of processors using the measured time as a time for ~~propagating~~ distributing the time synchronous signal ~~between two~~ to the plurality of processors in the multi-processor system, and synchronizing the timers of the plurality of processors.

2. (original) The timer adjusting system according to claim 1, wherein the generating circuit generates the time synchronous signal using a signal that is generated by one of the timers of the plurality of processors.

3. (currently amended) The timer adjusting system according to claim 1, wherein the measuring circuit measures the time for ~~propagating~~ distributing the time synchronous signal, using one of the timers of the plurality of processors.

4. (original) The timer adjusting system according to claim 1, wherein the synchronization circuit comprises:

a first software unit executing a software command for controlling a reference timer among the timers of the plurality of processors; and

a second software unit executing a software command for controlling a timer to be corrected, and

the synchronization circuit corrects time information of the timer to be corrected using time information of the reference timer and the measured time.

5. (original) The timer adjusting system according to claim 4, further comprising a generating circuit generating a start signal that starts a counting operation of the timer to be corrected when the input circuit inputs the time synchronous signal, wherein

the second software unit stops the timer to be corrected, stores the corrected time information in the timer to be corrected, and sets the timer to be corrected in a condition where a counting operation starts based on the start signal.

6. (currently amended) The timer adjusting system according to claim 5, wherein

the measuring circuit measures the time for ~~propagating~~ distributing the time synchronous signal at a time of reconfiguration of the multi-processor system with addition of a processor, and

the second software unit controls the timer of the processor to be added as the timer ~~of the processor~~ to be corrected.

7. (currently amended) The timer adjusting system according to claim 1

further comprising a storing circuit storing the measured time,

wherein the measuring circuit measures the time for ~~propagating~~ distributing the time synchronous signal at the time of initialization of the multi-processor system, and stores the measured time in the storing circuit, and

wherein the synchronization circuit obtains the stored time at the time of correction for a value in the timer to be corrected.

8. (original) A timer adjusting system adjusting timers of a plurality of processors in a multi-processor system, each of the plurality of processors comprising:

a generating circuit generating a time synchronous signal for the multi-processor system;

an output circuit outputting the time synchronous signal as a synchronous output; and

an input circuit inputting a synchronous input,

and the timer adjusting system comprising:

a distributing circuit generating a logical OR signal of a plurality of synchronous output output by the plurality of processors, and distributing the logical OR signal to the plurality of processors as the synchronous input;

a measuring circuit measuring a time while one of the plurality of processors outputs the synchronous output and receives the synchronous input; and

a synchronization circuit correcting time information of one or more timers of the plurality of processors using the measured time as a time for propagating the logical OR signal, and synchronizing the timers of the plurality of processors.

9. (original) The timer adjusting system according to claim 8, further comprising a control circuit dividing the multi-processor system into a plurality of partitions, and activating each partition as a symmetric multi-processor system, wherein

the distributing circuit generates a logical OR signal of synchronous outputs that are output from processors belonging to each partition, and distributes the logical OR signal to the processors belonging to each partition as a synchronous input, and

the synchronization circuit synchronizes timers of the processors belonging to each partition.

10. (currently amended) A timer adjusting system for adjusting timers of a plurality of processors in a multi-processor system, ~~comprising: generating means for~~ each processor generating a time synchronous signal for the multi-processor system,~~; output means for~~ outputting the time synchronous signal, and~~; input means for~~ inputting the time synchronous signal ~~that is output from the output means~~, said timer adjusting system comprising:

distributing means for propagating the time synchronous signal output from the output circuit of one of the processors to all of the processors in the multi-processor system and ~~returns~~ for returning the time synchronous signal to the input circuit of the one of the processors after being propagated in the multi-processor system;

measuring means for measuring a time ~~while~~ during which the ~~output means~~ one of the processors outputs the time synchronous signal and ~~the input means~~ inputs the time synchronous signal; and

synchronizing means for correcting time information of one or more timers of the plurality of processors using the measured time as a time for ~~propagating~~ distributing the time synchronous signal ~~between two~~ to the plurality of processors in the multi-processor system, and synchronizing the timers of the plurality of processors.

11. (original) A timer adjusting system adjusting timers of a plurality of processors in a multi-processor system, each of the plurality of processors comprising:

generating means for generating a time synchronous signal for the multi-processor system;

output means for outputting the time synchronous signal as a synchronous output; and

input means for inputting a synchronous input,

and the timer adjusting system comprising:

distributing means for generating a logical OR signal of a plurality of synchronous outputs output by the plurality of processors, and distributing the logical OR signal to the plurality of processors as the synchronous input;

measuring means for measuring a time while one of the plurality of processors outputs the synchronous output and receives the synchronous input; and

synchronizing means for correcting time information of one or more timers of the plurality of processors using the measured time as a time for propagating the logical OR signal, and synchronizing the timers of the plurality of processors.